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10/573,527	03/24/2006	Kiyoshi Kato	0756-7660	5487

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EXAMINER	
WOLDEGEORGIS, ERMIAS T	

ART UNIT	PAPER NUMBER
2893	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,527	KATO ET AL.	
	Examiner	Art Unit	
	ERMIAS WOLDEGEORGIS	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-9,11-13 and 15-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22* is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-9,11-13 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/13/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *NPL*

DETAILED ACTION

1. Response to amendment

Claims 3, 6, 10 and 14 have been cancelled; claims 1, 2, 4-5, 7, 9, 11-13, 15-16 and 21 have been amended; claim 22 has been newly added; and claims 1, 2, 4-5, 7-9, 11-13 and 15-22 are currently pending.

2. Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

3. Information Disclosure Statement

The information disclosure statement (IDS) filed on 1/13/2011 has been acknowledged and a signed copy of the PTO-1449 is attached herein.

4. Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 4-5, 7-9, 11-13 and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. **(US. 2002/0126108 A1, hereinafter "Koyama")**.

In regards to claims 1 and 7, Koyama discloses (Figs. 26(A)-27(B)) a memory device comprising a memory cell **(memory portion, Fig. 27(B))** formed over an insulating surface **(2602)**, which includes a semiconductor film **(2603-2606)** having two impurity regions **(for example 2636/2637)** a region therebetween **(the channel region of the semiconductor film)**, an insulating film **(2608)** over the semiconductor film **(2603-2606)**, a gate electrode **(for example 2617/2752)** formed over the region with the insulating film **(2608)** interposed therebetween, and at least two wirings **(for example 2767/2768)** connected to the respective impurity regions **(for example 2636/2637)**, wherein the semiconductor film **(2603-2606)** interposed between the two wirings **(for example 2767/2768)** of the memory cell **(memory portion, Fig. 27(B))** is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings **(since the material used for island shape semiconductor layer of the present application and the Koyama reference are the same: a-silicon, it is the property of this material to alter when applying voltage during operation and/or programming of the device. Therefore, a-silicon exhibits the same property as claimed here)**; and wherein the gate electrode **(for example 2617/2752)** has a gap **(the gap between the channel and the gate occupied by the gate insulating film)** over the region **(the channel region of the semiconductor film)**.

In regards to claims 4 and 11, Koyama discloses (Figures 26(A)-27(B)) a memory device comprising a first memory cell and a second memory cell (though a single memory sell is shown, it is apparent that plurality of memory cells are formed throughout the substrate) formed over an insulating surface **(2602)**, each of which includes a semiconductor film **(2603-2606)** having at least two impurity regions **(for example 2636/2637)** and a region therebetween **(the channel region of the semiconductor film)**, an insulating film **(2608)** on the semiconductor film **(2603-2606)**, a gate electrode **(for example 2617/2752)** formed over the region with the insulating film **(2608)** interposed therebetween, and two wirings **(2767/2768)** connected to the respective impurity regions **(2636/2637)**, wherein the first memory cell comprises an initial state **(inherently there at least one bit to tell whether data is stored or not)**; and the semiconductor film **(2606)** interposed between the two wirings **(2767/2768)** of the second memory cell **(2774)** is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings **(since the material used for island shape semiconductor layer of the present application and the Koyama reference are the same: a-silicon, it is the property of this material to alter when applying voltage during operation and/or programming of the device. Therefore, a-silicon exhibits the same property as claimed here)**, and wherein the gate electrode **(for example 2617/2752)** has a gap **(the gap between the channel and the gate occupied by the gate insulating film)** over the region **(the channel region of the semiconductor film)**.

In regards to claim 15, Koyama discloses (Figures 26(A)-27(B)) a manufacturing method of a memory device, comprising the steps of: forming an island shape semiconductor film **(2606)** over an insulating surface **(2602)**; forming a gate insulating film **(2608])** over the island shape semiconductor film **(2603-2606)**; forming a gate electrode **(for example 2617)** over the gate insulating film **(2608)**; doping an N-type impurity element **(Par [0284])** with the gate electrode **(2617)** used as a mask **(Par [0289-0290])**, thereby forming an N-type high concentration impurity region **(2637/2638)** in the island shape semiconductor film **(2603-2606)**; forming an interlayer film **(2761/2762)** over the gate insulating film **(2608)** and the gate electrode **(2617)**; forming a contact hole **(Par [0298])** in the interlayer film **(2761/2762)** and a wiring **(2767/2768)** connected to the N-type high concentration impurity region (**for example 2636/2637)**, thereby forming a memory cell **(memory 2774)**, and applying a voltage between the gate electrode and the wiring of the memory cell, thereby altering a channel region of the island shape semiconductor film to an insulating state **(since the material used for island shape semiconductor layer of the present application and the Koyama reference are the same: a-silicon, it is the property of this material to alter when applying voltage during operation and/or programming of the device. Therefore, a-silicon exhibits the same property as claimed here)**; and wherein the gate electrode **(for example 2617/2752)** has a gap **(the gap between the channel and the gate occupied by the gate insulating film)** over the island shape semiconductor film **(2603-2606)**.

In regards to claims 2, 5, 9, 13 and 16, Koyama discloses (Figs. 27A) the memory cell of the write-once memory device comprises two or more gate electrodes **(2617/2752)** on the same insulating film **(2608)** over the same semiconductor film **(for example 2606)**.

In regards to claims 8 and 12, Koyama discloses the gate electrode **(for example 2617/2752)** is interposed between the two wirings **(2767/2768)**.

6. Claims 17-21 are rejected under 35 U.S.C. 103(a) as unpatentable over Koyama in view of Zhao et al. **(IEEE ISBN 0-7803-1450-6, hereinafter "Zhao")**

In regards to claims 17-21, Koyama as modified above fails to explicitly teach sidewalls formed on side surfaces of the gate electrode.

Zhao while disclosing TFT device utilizing a polysilicon floating gate spacer (abstract) teaches (Fig. 1) sidewalls **(N+ floating gate poly spacer)** formed on side surfaces of the gate electrode **(N+ poly)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a polysilicon floating gate spacer on side surfaces of the gate electrode because as taught by Zhao in Page 15.4.1 and 15.4.2 (Abstract/Conclusion), it effectively reduces the OFF state leakage current and suppress the kin effect while maintaining a reasonable ON current.

7. Allowable Subject Matter

Claim 22 is allowed over prior art of record.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach, " a first memory cell ... two first impurity regions and a first region therebetween ...
a second memory cell ... two second impurity regions and a second region therebetween ... wherein the first region is altered to an insulating state and the second region is maintained in an initial state when applying a gate voltage to the first gate electrode and the second gate electrode, a first voltage to at least one of the two first wirings, and a second voltage to at least one of the two second wirings, and
wherein the first voltage is lower than the second voltage.", as recited in claim 22.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Response to Arguments

Applicant's arguments with respect to claims 1, 4, 7, 11 and 15 have been considered but are moot in view of the new ground(s) of rejection.

9. Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is

(571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 6:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/
Examiner, Art Unit 2893

/A. Sefer/
Primary Examiner
Art Unit 2893